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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,852	03/12/2004	Isamu Miyanishi	2271/71532	2074
7590 Ivan S. Kavrukov, Esq. Cooper & Dunham LLP 1185 Avenue of the Americas New York, NY 10036			EXAMINER ZAMAN, FAISAL M	
			ART UNIT 2111	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/799,852

Applicant(s)

MIYANISHI ET AL.

Examiner

Faisal M. Zaman

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 January 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 22-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/06)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 39 and 40** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Each of the claims depend on a cancelled claim (i.e., Claim 19), and thus are indefinite. For purposes of evaluating the claims with respect to the prior art, the examiner will presume that claims 39 and 40 depend on independent claim 22.

Appropriate corrections are therefore required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 22, 31, and 41** are rejected under 35 U.S.C. 102(b) as being anticipated by Horie (U.S. Patent No. 5,732,050).

Regarding Claims 22 and 31, Horie discloses an optical disk drive apparatus (Figure 1, item 12), comprising:

An optical disk drive mechanism (Figure 1, item 2) configured to read data from an optical disk medium (Figure 1, item 1);

A register circuit (Figure 1, item 5, Column 5, lines 34-38) including a plurality of registers configured to store data read by said optical disk drive mechanism from said optical disk medium to be transferred from the optical disk drive apparatus to a host computer (Figure 1, item 11);

A first memory configured to store first information indicating specific addresses of corresponding specified registers in the register circuit and representing an access executed by the host computer to the optical disk drive mechanism for a data transfer (Figure 1, item 8d, Column 7, lines 3-6);

A second memory configured to store second information, received by said second memory in association with the first information stored in the first memory and corresponding to said data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer, to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory (Figure 1, item 4, Column 7, lines 34-39);
and

A control circuit configured to perform an information writing operation for writing the first information and the second information into the first memory and the second memory, respectively, in chronological order of accesses executed (Column 7, lines 31-34; i.e., sector by sector), in connection with said data read by said optical disk drive

mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer (Figure 1, item 3, Column 7, lines 31-39),

Wherein the first memory stores first information indicating specific addresses of corresponding specified registers in the register circuit (Column 7, lines 3-6), and the second memory stores second information corresponding to said data read by said optical disk drive mechanism from said optical disk medium, to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory (Column 7, lines 34-39).

Regarding Claim 41, Horie discloses wherein the control circuit is configured to perform an information reading operation to read the first information and second from the first and second memories, respectively, and transfer and store the second information in the register indicated by the corresponding first information (Column 7, lines 31-39).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 23, 24, 30, 32, and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie and Chu et al. ("Chu") (U.S. Patent Application Publication No. 2004/0015731).

Regarding Claim 23, 24, 32, and 33, Horie does not expressly disclose wherein the control circuit performs the information writing and reading operation for writing and reading the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode.

In the same field of endeavor (e.g., reading data from an optical disk drive), Chu teaches wherein a control circuit performs the information writing and reading operation for writing and reading the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode (paragraph 0033; i.e., HDD 300 state is changed from eData mode to Active mode).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Chu's teachings of reading data from an optical disk drive with the teachings of Horie, for the purpose of reducing the power consumption in the computer system.

Regarding Claim 30, Chu discloses wherein the register circuit, the first and second memories, and the control circuit are integrated into a single integrated chip (Figure 3, item 301).

The motivation that was used in the combination of Claim 24, super, applies equally as well to Claim 30.

7. **Claims 25, 26, 29, and 34-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie and Chu as applied to Claims 22 and 31 above (hereinafter "Horie-Chu"), and further in view of Yamada et al. ("Yamada") (U.S. Patent No. 6,470,439).

Horie-Chu discloses the invention substantially as claimed.

Regarding Claims 25 and 35, Horie-Chu discloses wherein the control circuit conducts the information writing operations with respect to the first and second memories in synchronism with each other and conducts the information reading operations with respect to the first and second memories in synchronism with each other (Chu, paragraph 0033).

In same field of endeavor (e.g., the use of a memory control circuit in controlling memory used in various electronic devices), Yamada teaches the following limitation, which Chu does not expressly disclose:

Wherein a memory comprises a first-in and first-out memory (Yamada, title, abstract) including a specific number of buffer areas into which data from an external device is written (Yamada, Column 3, lines 18-31).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Yamada's teachings of the use of a memory control circuit in controlling memory used in various electronic devices with the teachings of Horie-Chu, for the purpose of providing a FIFO memory control circuit in which the amount of effective data in a memory can be correctly counted so that when the frequencies of a read clock and a write clock are different, data is prevented from being lost by being overwritten, and data is prevented from being read out twice (see Yamada, Column 6, lines 18-22).

Regarding Claims 26 and 36, Horie-Chu discloses wherein the control circuit performs the information writing and reading operation for writing and reading the first information into the first memory and the second information into the second memory in chronological order of accesses executed when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode (Chu, paragraph 0033; i.e., HDD 300 state is changed from eData mode to Active mode).

Horie-Chu does not expressly disclose wherein the information writing and reading operation is performed without buffering the first and second information in the first-in and first-out memories in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information stored in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when the

operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode.

In the same field of endeavor, Yamada teaches wherein data is not written (ie. is not buffered) into a FIFO memory in the event that a FULL signal is sent from the memory control circuit, indicating the FIFO memory is full (Yamada, Column 4, lines 12-22).

The motivation that was utilized in the combination of Claim 25, super, applies equally as well to Claims 26 and 36.

Regarding Claims 29 and 34, Yamada discloses the following, which Horie-Chu does not expressly disclose:

Wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for the information reading operation (Yamada, Column 3, lines 26-31), and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal (Yamada, Column 4, lines 43-52).

The motivation that was utilized in the combination of Claim 25, super, applies equally as well to Claims 29 and 34.

8. **Claims 27-28 and 37-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie-Chu and Yamada as applied to Claims 25 and 35 above

(hereinafter "HCY"), and further in view of Chuang et al. ("Chuang") (U.S. Patent No. 6,502,159).

HCY discloses the communications interface apparatus according to Claim 26, as described above.

Regarding Claims 27 and 37, HCY does not expressly disclose wherein each of the first and second memories comprises a selection circuit configured to select one of (i) a first data path for the first and second information not via the first and second memories and (ii) a second data path for the first and second information via the respective first and second memories, on an exclusive basis according to a control signal from the control circuit and to output corresponding data to the register circuit through the selected one of the first and second data paths.

In the same field of endeavor (e.g. data transfers between a disk drive apparatus and a host computer), Chuang teaches wherein a circuit (Chuang, Figure 2, item 105, Column 4, lines 22-23) comprises a selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) configured to select one of (i) a first data path for information not via a memory (Chuang, Table 2, Column 4, lines 26-29) and (ii) a second data path for the information via a memory (Chuang, Table 1, Column 4, lines 23-25), on an exclusive basis according to a control signal from a control circuit (Chuang, Figure 2, item 12, Column 3, lines 56-60) and to output corresponding data to a circuit (Chuang, Figure 3, item 57, Column 3, lines 56-60) through the selected one of the first and second data paths.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Chuang's teachings of data transfers between a disk drive apparatus and a host computer with the teachings of HCY, for the purpose of greatly reducing system memory usage and bus utilization (see Chuang, Column 3, lines 52-55) and to reduce unnecessary data flow in the system and unnecessary consumption of system resources (see Chuang, Column 3, lines 60-64).

Regarding Claims 28 and 38, HCY discloses wherein the control circuit comprises:

A data writing circuit block configured to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer (Chu, Figure 3, item 400);

A data reading circuit block configured to start reading the first and second information from the first and second memories, respectively, upon a time the write control circuit block starts writing the first and second information into the first and second memories, respectively (Chu, Figure 3, item 400);

A status detecting circuit block configured to detect memory statuses of the first-in and first-out memories included in the respective first and second memories and to output a status signal representing the memory statuses detected (Chu, Figure 3, item 338); and

A selection control circuit block configured to control accesses to the respective first and second memories in accordance with a status as to whether the operation

mode of the communications interface apparatus is the low power consumption mode and the status signal output from the status detecting circuit block (Chu, paragraphs 0032-0033; i.e., data from host 1 is only buffered in write cache 130 [Figure 2] or RAM 420 [Figure 3] when the HDD 300 is in eData [i.e., idle] mode).

HCY does not expressly disclose wherein the selection control circuit block is configured to control the selection circuits included in the respective first and second memories.

In the same field of endeavor, Chuang teaches wherein a selection control circuit block (Chuang, Figure 2, item 105, Column 4, lines 22-23) is configured to control the selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) included in a circuit in accordance with a status from a control circuit (Chuang, Figure 2, item 12, Column 3, lines 56-60).

The motivation used in the combination of Claim 27, super, applies equally as well to Claims 28 and 38.

9. **Claims 39 and 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie and Mirov et al. ("Mirov") (U.S. Patent No. 6,528,974).

Regarding Claim 39, Mirov teaches the following limitation, which Horie does not expressly teach: wherein in a regular operation mode, a first clock signal of a first frequency of said predetermined value is supplied from the clock generator to a data processor (Mirov, Figure 1, item 104), and in said low power consumption mode, a

second clock signal of a second frequency of said non-zero value is supplied from the clock generator to the data processor (Mirov, Column 4, lines 24-41).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Mirov's teachings of reading data from a disc for use by a computer to the teachings of Horie, for the purpose of providing a disc apparatus having a reduced power consumption during a sleep mode for greater efficiency in a computing system.

Regarding Claim 40, Mirov teaches wherein the clock generator includes a clock generation circuit configured to generate concurrently a plurality of clock signals of respective non-zero frequencies, and one of said plurality of clock signals of respective non-zero frequencies is selected to be output as said clock signal of said clock generator (Mirov, Column 5, lines 21-45).

The motivation that was used in the combination of Claim 39, *super*, applies equally as well to Claim 40.

Prior Art of Record

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Norman et al. (U.S. Patent No. 6,320,815 B1) discloses a memory system having flexible bus structure and method. Hayashi (U.S. Patent No. 6,487,616 B1) discloses a controller for a data recorder. Okazaki et al. (U.S. Patent No. 7,079,458 B2) discloses a buffer memory address translation device.

Response to Arguments

11. Applicant's arguments with respect to claims 22 and 31 have been considered but are moot in view of the new ground(s) of rejection. Horie (U.S. Patent No. 5,732,050) teaches all of the limitations of the argued claims, as discussed above.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal M. Zaman whose telephone number is (571)272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays, alternate Fridays off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/F. M. Z./
Examiner, Art Unit 2111

/MARK RINEHART/
Supervisory Patent Examiner, Art Unit 2111